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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/029,608	05/15/98	FUKASAWA	N 980233

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DATE MAILED: 04/30/01

Please find below and/or attached an Office communication concerning this application or proceeding.

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PTO-90C (Rev. 2/95)

1- File Copy

*U.S. GPO: 2000-473-000/44602

Office Action Summary	Application No. 09/029,608	Applicant(s) FUKASAWA ET AL.	
	Examiner David E Graybill	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2001* .

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18,19,36,41-43,54-64,70-77,79-85,87-91 and 95-107* is/are pending in the application.

4a) Of the above claim(s) *103-107* is/are withdrawn from consideration.

5)☒ Claim(s) *70,72-77,80,84,85,95 and 96* is/are allowed.

6)☒ Claim(s) *18,19,36,41-43,54-64,71,79,81-83,87-91 and 97-102* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☐ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

The request filed on 2-20-01 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/029,608 is acceptable and a CPA has been established. An action on the CPA follows.

Prosecution is being continued on the invention elected and prosecuted by applicant in the prior application.

In the following rejections, reference labels are not necessarily recited for other than the first recitation of identical claim language.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 18, 19, 36, 41, 43, 57-64, 71, 79, 81-83, 87-91 and 97-102 are rejected under 35 U.S.C. 102(e) as being anticipated by Kata (5897337).

At column 4, line 8 to column 14, line 50, Kata teaches the following:

18. A semiconductor device comprising: a semiconductor element 50 having a surface on which electrode pads 41 connected to an internal part of the semiconductor element and protruding electrodes 66 to be connected to an external part are formed; lead lines 62 each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines; and a resin layer 61/43 which is formed on the surface of the semiconductor element and seals at least a lateral surface of the protruding electrodes; wherein the lead lines are located between the semiconductor element and the resin layer.

19. The semiconductor device as claimed in claim 18, further comprising a heat radiating member 46 provided on a back surface of the semiconductor element opposite to the surface thereof on which the protruding electrodes are provided.

36. A semiconductor device comprising: a semiconductor element having a surface on which electrode pads connected to an internal part of the semiconductor element and external connection electrodes are provided which are to be electrically connected to external terminals; lead lines each connecting one of the electrode pads and one of the external connecting

electrodes so that the external connecting electrodes and the internal part are connected through the lead lines; and

a resin layer provided on the surface of the semiconductor element so as to cover the external connection electrodes, wherein the external connection electrodes are exposed at a lateral surface of the resin layer and the lead lines are located between the semiconductor element and the resin layer.

41. The semiconductor device as claimed in claim 18, wherein the resin layer comprises a plurality of resin layers having different characteristics.

43. A semiconductor device comprising: a semiconductor element having a surface on which electrode pads connected to an internal part of the semiconductor element and protruding electrodes to be connected to an external part are formed; lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected, through the lead lines; a resin layer which is formed on the surface of the semiconductor element and seals lateral surfaces of the protruding electrodes; and external connection protruding electrodes 67 provided to the ends of the protruding electrodes exposed from the resin layer;

wherein the lead lines are located between the semiconductor element and the resin layer.

57. A semiconductor device comprising: a plurality of semiconductor elements 41; a compressed sealing resin 43 which seals partially or totally the semiconductor elements; and an electrode plate 60' which is provided in the compressed sealing resin and is electrically connected to the semiconductor elements, the electrode plate having portions 62' which are exposed from side surfaces of the compressed sealing resin and function as external connection electrodes.

58. The semiconductor device as claimed in claim 57, wherein the semiconductor elements are connected to the electrode plate in a flip-chip bonding formation.

59. The semiconductor device as claimed in claim 57, wherein the electrode plate is exposed from a bottom surface of the sealing resin in addition to the side surfaces thereof, so that portions 62' of the electrode plates exposed from the bottom surface function as external connection terminals.

60. The semiconductor device as claimed in claim 57, wherein protruding terminals 71-1 are provided to the electrode plate, and are exposed from a bottom surface of the sealing resin, so

that the protruding terminals function as external connection terminals.

61. The semiconductor device as claimed in claim 60, wherein the protruding terminals are portions of the electrode plate defined by plastic deformation.

62. The semiconductor device as claimed in claim 60, wherein the protruding terminals are protruding electrodes arranged to the electrode plate.

63. The semiconductor device as claimed in claim 57, wherein the semiconductor elements are partially exposed from the sealing resin.

64. The semiconductor device as claimed in claim 57, further comprising a heat radiating member 60' in a position close to the semiconductor elements.

71. A mounting arrangement for mounting a semiconductor device on a mounting board, the semiconductor device comprising: a plurality of semiconductor elements 41; a compressed sealing resin 43 which seals partially or totally the semiconductor elements; an electrode plate 60' which is provided in the sealing resin and is electrically connected to the semiconductor elements, the electrode plate having portions 62' which are exposed from side surfaces of the compressed sealing resin and

function as external connection electrodes: and protruding terminals 67 provided to the electrode plate, and exposed from a bottom surface of the compressed sealing resin, so that protruding terminals function as external connection terminals; the mounting arrangement comprising: bumps 67 arranged to the protruding terminals for forming the external connection terminals, the semiconductor device being connected to the mounting board through the bumps.

79. A semiconductor device comprising: a semiconductor device main body 14 having a semiconductor element having a surface on which protruding electrodes are directly formed, and a compressed resin layer 44 which is formed on the surface of the semiconductor element and seals lateral surfaces of the protruding electrodes; an interposer 26 to which the semiconductor device main body is attached, the interposer being attached to a side [the top side] of the protruding electrodes of the semiconductor main body, a wiring pattern 30 to which the semiconductor device main body is connected being formed on a base member 28 of the interposer; an adhesive which is provided between the semiconductor device main body and the interposer and which bonds the semiconductor device main body to the interposer; a conductive member 40 which electrically connects

the semiconductor device main body and the interposer; and external connection terminals 12 which are connected to wiring pattern through holes formed in the base member and are arranged on a surface of the semiconductor device main body opposite to the surface on which the protruding electrodes are provided.

81. The semiconductor device as claimed in claim 79, wherein the conductive member comprises stud bumps.

82. The semiconductor device as claimed in claim 79, wherein the conductive member comprises flying leads, which are integrally formed with the wiring pattern and bypasses the adhesive so as to be connected to the protruding electrodes.

83. The semiconductor device as claimed in claim 82, wherein connections of the protruding electrodes and the flying leads are sealed by resin.

87. A semiconductor wafer on which semiconductor elements are provided, comprising: a semiconductor wafer 50 including a plurality of semiconductor elements having a surface on which electrode pads connected to an internal part of the semiconductor elements and protruding electrodes to be connected to an external part are formed; lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are

connected through the lead lines and a resin layer which is formed on the surface of the semiconductor elements and seals at least a lateral surface of the protruding electrodes; wherein the lead lines are located between the semiconductor elements and the resin layer.

(88). A semiconductor device comprising: a semiconductor element having a surface on which, electrode pads connected to an internal part of the semiconductor element and protruding electrodes to be connected to an external part ate formed; lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines; and a resin layer which is formed on the surface of the semiconductor element and seals at least a lateral surface of the protruding electrodes, wherein a lateral surface of the resin layer and a lateral surface of the semiconductor element have planes cut by a dicer, and the lead lines are located between the semiconductor element and the resin layer.

(89). A semiconductor device as claimed in claim 88, wherein the lateral surface of the resin layer and the lateral surface of the semiconductor element have a common plane cut by a dicer.

90. A semiconductor device comprising: a semiconductor element having a surface on which external connection electrodes are provided, which are to be electrically connected to external terminals; and a compressed resin layer provided on the surface of the semiconductor elements so as to cover the external connection electrodes, wherein the external connection electrodes are exposed at a lateral surface of the compressed resin layer, the lateral surface of the resin layer and the lateral surface of the semiconductor element have planes cut by a dicer.

91. A semiconductor device comprising: a semiconductor element having a surface on which electrode pads connected to an internal part of the semiconductor element and protruding electrodes to be connected to an external part are formed; lead lines each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines; and a resin layer which is formed on the surface on the semiconductor element and seals a lateral surface and a top of the protruding electrodes, the resin layer slightly covering upper portions of the protruding electrodes; wherein the lateral surface of the resin layer and the lateral surface of the semiconductor element

have planes cut by a dicer and the lead lines are located between the semiconductor element and the resin layer.

97. The semiconductor device as claimed in claim 88, wherein the [compressed] resin layer is formed by disposing a film between the protruding electrodes and a mold, which thus contacts the resin layer through the film.

98. The semiconductor device as claimed in claim 88, wherein a sheet-shaped resin is used as the resin layer.

99. The semiconductor device as claimed in claim 88, wherein a reinforcement plate is loaded onto a mold before the substrate is loaded onto the mold in forming the resin layer.

100. The semiconductor device as claimed in claim 88, wherein: a film used in forming the resin layer is formed of an elastically deformable substance, and ends of the protruding electrodes are caused to fall in the film when the resin layer is formed by using a mold; and the film is detached from the resin layer when the protruding electrodes are exposed so that the ends of the protruding electrodes can be exposed from the resin layer.

102. The semiconductor device as claimed in claim 88, wherein the resin layer comprises a plurality of sealing resins having different characteristics.

To further clarify the teaching of a plurality of resin layers having different characteristics, it is noted that the layers have different location characteristics.

To further clarify the teaching of a compressed resin layer 43, it is noted that Kata teaches this product at column 8, lines 23-24; and column 9, lines 37-43 because the resin layer is inherently compressed when the film is pressed.

To further clarify the teaching of a resin layer 43 which seals a top of the protruding electrodes, it is noted that the resin layer seals a top of the lateral surface of the electrode. In any case, there is no absolute frame of reference recited; therefore, it is inherent that for any particular sealed portion of the electrode, an absolute frame of reference can be chosen in which the portion is a top of the electrode.

To further clarify the teaching of the resin layer slightly covering upper portions of the protruding electrodes, attention is directed to figure 8D wherein the resin layer slightly covers the upper portions of the protruding electrodes that slightly overlap the external surface of the layer.

Also, although Kata does not appear to explicitly teach the process limitations of claims 81, 88-91, 97, 99 and 100, the product of Kata inherently possesses the structural

characteristics imparted by the limitations. See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

Claim 42 is rejected under 35 U.S.C. 102(b) as being anticipated by Kata (5683942).

At column 3, line 34 to column 10, line 47, Kata teaches the following:

(42) A semiconductor device comprising: a semiconductor element 1 having a surface on which electrode pads 2 connected to an internal part of the semiconductor element and protruding electrodes 4/9 to be connected to an external part are formed; lead lines 6 each connecting one of the electrode pads and one of the protruding electrodes so that the protruding electrodes and the internal part are connected through the lead lines, and a first resin layer 3 that is formed on the surface of the semiconductor element and seals lateral surfaces of the protruding electrodes; and a second resin layer 53 provided so as to cover at least a back surface of the semiconductor element; wherein the lead lines are located between the semiconductor element and the resin layers.

Claims 54-56 are rejected under 35 U.S.C. 102(e) as being anticipated by Kitahara (5568363).

At column 5, line 25 to column 16, line 34 Kitahara teaches the following:

54. A semiconductor device comprising: a semiconductor element 1; protruding electrodes ("circular-arc form") functioning as external connection terminals; a wiring board 4 having a flexible base 41 on which leads 3 are formed, the leads having ends 31 connected to the semiconductor element and other ends 32 connected to the protruding electrodes and the flexible base having a cavity in which the semiconductor element is placed; and a sealing resin 2 sealing the semiconductor element, wherein there are provided extending portions 3 that are formed to the wiring board so that the extending portions laterally extend from a position in which the semiconductor element is placed, the protruding electrodes being formed on the extending portions.

55. The semiconductor device as claimed in claim 54, further comprising a frame 95 which supports the wiring board and which has a cavity which accommodates the semiconductor element.

56. The semiconductor device as claimed in claim 54, wherein the protruding electrodes are mechanical bumps obtained by plastic deforming the leads.

Claims 70, 72-77, 80, 84, 85, 95 and 96 are allowed.

Applicant's amendment and remarks filed 1-22-01 are addressed in the rejection supra and are further addressed infra.

Applicant's identification of the pending claims is incomplete because claims 104-107 are also pending.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to the group receptionist whose telephone number is 703-308-1782.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/305-3431.

David E. Graybill
Primary Examiner
Art Unit 2814

D.G.
26-Apr-01